Amendments to the Drawings:

The attached sheet of drawing includes changes to Fig. 4. This sheet, which includes Fig. 4, replaces the original sheet including Fig. 4, in which the ordinate has been labeled "ON Current Change Ratio" and the abscissa has been labeled as "Stress Time (Sec)".

Attachment: Replacement Sheet

Annotated Sheet Showing Changes

REMARKS

By the above amendment, claims 15 - 20 which stand withdrawn from consideration as being directed to a non-elected invention have been canceled without prejudice or disclaimer of the subject matter thereof and without prejudice to the right to file a divisional application directed thereto.

The indication that claims 3 - 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form is acknowledged. By the present amendment, claim 3 has been written in independent form while clarifying features with minor amendments being effected in dependent claims thereof such that applicants submit that claims 3 - 14 should now be in condition for allowance.

Also, by the present amendment, claim 1 has been amended to incorporate features of dependent claims 3 therein, which features the Examiner recognizes are not disclosed in the cited art, such that applicants submit that claim 1 as amended and the dependent claims should also be in condition for allowance. It is noted that claim 2 has been rewritten in independent form and amended to clarify features thereof and new dependent claims 21 - 25, which depend directly or indirectly from claim 1 have been presented, and which recite further features of the present invention, as will be discussed below.

With regard to the objection to the drawing because Fig. 4 has no units, submitted herewith is a replacement sheet of drawing of Fig. 4 in which the ordinate has been labeled "ON Current Change Ratio" and the abscissa has been labeled as "Stress Time (Sec)", as described in the specification of this application. Thus, applicants submit that the objection to the drawing should now be overcome and acceptance of the drawings is respectfully requested.

As to the rejection of claim 1 under 35 USC 102(e) as being anticipated by Yamazaki et al, this rejection is traversed insofar as it is applicable to the present claims and reconsideration and withdrawal of the rejection are respectfully requested.

Applicants note that the office action of November 3, 2005 does not set forth a rejection under 35 USC 102 or 35 USC 103 of claim 2.

As to the requirements to support a rejection under 35 USC 102, reference is made to the decision of In re Robertson, 49 USPQ 2d 1949 (Fed. Cir. 1999), wherein the court pointed out that anticipation under 35 U.S.C. §102 requires that each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. As noted by the court, if the prior art reference does not expressly set forth a particular element of the claim, that reference still may anticipate if the element is "inherent" in its disclosure. To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Moreover, the court pointed out that inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.

With respect to claim 1, as amended, claim 1 now recites a feature, as previously recited in claim 3, and considered allowable by the Examiner, that the carbon concentration of the gate insulation film at the side close to the semiconductor layer is equal to or less than 1/10 the carbon concentration at the side remote from the semiconductor layer. That is, as noted by the Examiner, "No prior art discloses the claimed invention with a specific ratio of carbon concentration

between the interface with the semiconductor layer and the interface at a site remote from the semiconductor layer". Accordingly, applicants submit that claim 1, as amended, patentably distinguishes over Yamazaki et al in the sense of 35 USC 102 and should be considered allowable thereover.

With respect to claim 2 which has been written in independent form and features thereof clarified, claim 2, for which no stated ground of rejection appears in the office action, has been amended to clarify the structural arrangement as illustrated in Fig. 2B of the drawings of this application, for example, wherein the gate insulation film includes at least one layer of deposition film (GI) which is deposited by a deposition method (GI), and an other layer (GI(H))which is formed by other than a deposition method and is interposed between the at least one layer of deposition film and the semiconductor layer, and the carbon concentration of the one deposition film layer has the distribution in which the carbon concentration is smaller at a site close to the semiconductor layer than at a site remote from the semiconductor layer. Referring to Yamazaki et al and Fig. 9 thereof, as described at column 11, lines 15 - 20, on the channel forming region (809), a gate wiring is formed through a laminated film of a first gate insulating film (203b) and a second gate insulating film (203c). As described at column 11, lines 58 - 63, in the structure of the invention, the concentration of the impurities such as carbon at the interface between the channel forming region (809) and the first gate insulating film (203b) is lower than the concentration of the impurity at the interface between the first gate insulating film (203b) and the second gate insulating film (203c). Thus, as shown in Fig. 9, the first gate insulating film (203b) is disposed between the channel forming region (809) and the second gate insulating film (203c), and as described at column 12, lines 38 - 40, the first gate insulating film (203b) is formed by a CVD method, i.e., a deposition

method. It does not appear that Yamazaki et al describes the manner of formation of the second gate insulating film (203c). In any event, it is readily apparent that while Yamazaki et al discloses a two layer structure of the gate insulating film (203b and 203c), it is readily apparent that Yamazaki et al does not disclose in the sense of 35 USC 102 or in the sense of 35 USC 103 the recited features of claim 2, as amended, wherein a layer of the gate insulation film formed by other than a deposition method is interposed between the layer of the gate insulation film formed by the deposition method and the semiconductor layer, and that the layer of the deposition film has the carbon concentration distribution as recited. Thus, applicants submit that claim 2 patentably distinguishes over Yamazaki et al in the sense of 35 USC 102 and 35 USC 103 and should be considered allowable thereover.

With respect to newly added claims 21 - 25, such claims recite further features of the present invention and depend directly or indirectly from claim 1, which should be considered allowable, as pointed out above. Thus, these claims should also be considered allowable at this time.

In view of the above amendments and remarks, applicants submit that all claims present in this application should now be in condition for allowance and issuance of an action of favorable nature is courteously solicited.

To the extent necessary, applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli,

Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case: 501.43513X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

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FIG. 4